REMARKS

Claims 1-24 are presently active.

In the Office Action dated 20 October 2003 ("Office Action"), claims 1, 15, and 24 were rejected under 35 U.S.C. §102(a) as being anticipated by Applicants' admitted prior art (Fig. 1); claims 2-7 and 16-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicants' admitted prior art (Fig. 1); and claims 8-14 and 21-23 were allowed.

Applicants acknowledge with appreciation the allowance of claims 8-14 and 21-23.

35 U.S.C. §102(a) rejection of claims 1, 15, and 24

To better define the invention, claim 1 is amended to recite that the NAND gate has a first input port directly connected to the node. As indicated in the Office Action, page 5, it was indicated that claim 1 would be allowable if "directly" was inserted. Accordingly, it is believed that claim 1 should be allowable.

Claim 24 is amended similarly. Also, claim 24 is amended to correct an antecedent basis problem, whereby "logic gate" is amended to read "NAND gate". Accordingly, claim 24 is believed to be allowable.

Because claim 15 depends upon claim 1, it to is believed allowable.

These and other claims have also been amended to insert "directly" before "connected", so that the invention is better defined.

35 U.S.C. §103(a) rejection of claims 2-7 and 16-20

Claims 2-4, 16, and 17 depend upon claim 1, and therefore with the amendment of claim 1, these claims should be allowable.

To better define the invention, claim 5 is amended to recite a CMOS static NAND gate. For a CMOS static NAND gate, there is a nMOSFET for every pMOSFET, where the configuration of the nMOSFETs is complementary to the configuration of the pMOSFETs. See, for example, The IEEE Handbook, ed. R. C. Dorf, IEEE and CRC Press, 1993, page 1617, where it is stated that "COMOS NAND gates are constructed by

paralleling p-channel MOSFETs, one for each input, and putting in series an n-channel MOSFET for each input, as shown in the block diagram of Fig. 73.3."

In light of the above description of NAND gates according to the IEEE Handbook, the combination of pMOSFETs 112 and 114 in Fig. 1 of the present application should not be identified as a CMOS static NAND gate. Accordingly, claim 5, and claims 6, 7, and 18-20 which depend upon claim 5, are believed patentable over Fig. 1 of the present application.

Respectfully submitted,

Seth Z Kalson Dated: 3-17-04

Seth Z. Kalson
Reg. no. 40,670
Attorney for Applicant(s) and Intel Corporation (Assignee)